

AMENDMENT(S) TO THE CLAIMS

1. (previously presented): An integrated circuit, comprising:
one or more components, including a feedback component, that receive a distributed voltage, wherein the feedback component of the one or more components has substantially similar input characteristics to at least one other component of the one or more components; and

a voltage driver that produces a compensated voltage;

wherein the compensated voltage is distributed to form the distributed voltage at the one or more components, and the distributed voltage is degraded relative to the compensated voltage; and

wherein the voltage driver is responsive to feedback from the feedback component as derived from the distributed voltage to adjust the compensated voltage so that the distributed voltage is approximately equal to a nominal voltage.

2. (original): An integrated circuit as recited in claim 1, wherein said one or more components have input characteristics that contribute to the degradation of the distributed voltage.

3. (original): An integrated circuit as recited in claim 1, wherein said distribution contributes to the degradation of the distributed voltage.

1 4. (original): An integrated circuit as recited in claim 1, wherein:
2 said distribution contributes to the degradation of the distributed voltage;
3 and
4 the compensated voltage is distributed over impedance-matched conductors
5 to form the distributed voltage at the one or more components.

6
7 5. (previously presented): An integrated circuit as recited in claim 1,
8 wherein said one or more components, excepting the feedback component,
9 comprise data receivers that evaluate data signals relative to the distributed
10 voltage.

11
12 6. (previously presented): An integrated circuit as recited in claim 1,
13 wherein the feedback component evaluates the distributed voltage relative to the
14 nominal voltage to derive said feedback.

15
16 7. (previously presented): An integrated circuit as recited in claim 1,
17 wherein:

18 the substantially similar input characteristics of the one or more
19 components contribute to the degradation of the distributed voltage; and

20 the feedback component evaluates the distributed voltage relative to the
21 nominal voltage to derive said feedback, wherein the substantially similar input
22 characteristics contribute similar degradation to the distributed voltage at the one
23 or more components.

1 **8.** (previously presented): An integrated circuit as recited in claim 1,
2 wherein:

3 the feedback component evaluates the distributed voltage relative to the
4 nominal voltage to derive said feedback;

5 said distribution contributes to the degradation of the distributed voltage;
6 and

7 the distributed voltage is routed to result in similar degradations at the one
8 or more components.

9
10 **9.** (previously presented): An integrated circuit as recited in claim 1,
11 wherein:

12 the feedback component evaluates the distributed voltage relative to the
13 nominal voltage to derive said feedback; and

14 the voltage driver has a variable gain that is configured to increase in
15 response to the feedback when the distributed voltage is less than the nominal
16 voltage and to decrease in response to the feedback when the distributed voltage is
17 greater than the nominal voltage.

18
19 **10.** (original): An integrated circuit as recited in claim 1, wherein the
20 voltage driver has a variable gain that is controlled by a digital value.

1 **11.** (original): An integrated circuit as recited in claim 1, wherein the
2 voltage driver has a variable gain that is controlled by a digital value, the
3 integrated circuit further comprising a register that is configurable to store the
4 digital value and to provide the digital value to the voltage driver.

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6 **12.** (original): An integrated circuit as recited in claim 1, wherein the
7 voltage driver has a variable gain that is controlled by a digital value, the
8 integrated circuit further comprising a register that is configurable to store the
9 digital value and to provide the digital value to the voltage driver, the register
10 being readable and writable.

11
12 **13.** (original): An integrated circuit as recited in claim 1, wherein the
13 voltage driver has a variable gain that is controlled by a digital value, further
14 comprising a counter that produces the digital value, wherein the counter is
15 responsive to the feedback to increment and decrement the digital value.

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17 **14.** (previously presented): An integrated circuit as recited in claim 1,
18 wherein the voltage driver has a variable gain that is controlled by a digital value,
19 further comprising a counter that produces the digital value, wherein the counter is
20 responsive to the feedback during an initialization period to increment and
21 decrement the digital value, and the digital value remains constant during an
22 operational period following the initialization period.

1 15. (original): An integrated circuit as recited in claim 1, wherein the
2 integrated circuit comprises a memory device.

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4 16. (original): An integrated circuit as recited in claim 1, wherein the
5 integrated circuit is a memory device that further comprises a plurality of memory
6 storage cells.

7
8 17. (previously presented): An integrated circuit, comprising:
9 one or more data receivers that evaluate one or more corresponding data
10 signals relative to a distributed reference voltage;
11 a feedback receiver that evaluates the distributed reference voltage relative
12 to a nominal reference voltage to produce a feedback signal; and
13 a reference voltage driver that produces a compensated reference voltage;
14 wherein the compensated reference voltage is distributed to form the
15 distributed reference voltage, and the distributed reference voltage is degraded
16 relative to the compensated reference voltage;
17 wherein the reference voltage driver has a variable gain that increases when
18 the distributed reference voltage is less than a nominal reference voltage and
19 decreases when the distributed reference voltage is greater than the nominal
20 reference voltage responsive to the feedback signal; and
21 wherein the feedback receiver and at least one data receiver of the one or
22 more data receivers have substantially similar input characteristics.

1 **18.** (original): An integrated circuit as recited in claim 17, wherein the
2 reference voltage driver is configured so that its gain is set during an initialization
3 period and remains constant during a subsequent operational period.
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5 **19.** (original): An integrated circuit as recited in claim 17, wherein the
6 variable gain is controlled by a digital value.
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8 **20.** (previously presented): An integrated circuit as recited in claim 17,
9 wherein the variable gain is controlled by a digital value, and the integrated circuit
10 further comprises a register that is configurable to store the digital value and to
11 provide the digital value to the reference voltage driver.
12

13 **21.** (previously presented): An integrated circuit as recited in claim 17,
14 wherein the variable gain is controlled by a digital value, and the integrated circuit
15 further comprises a register that is configurable to store the digital value and to
16 provide the digital value to the reference voltage driver; and wherein the register is
17 readable and writable.
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19 **22.** (original): An integrated circuit as recited in claim 17, wherein the
20 variable gain is controlled by a digital value, further comprising a counter that
21 produces the digital value, wherein the counter increments or decrements the
22 digital value depending on the relationship of the distributed reference voltage
23 relative to the nominal reference voltage.
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1 **23.** (Previously presented): An integrated circuit as recited in claim 17,
2 wherein the variable gain is controlled by a digital value, and the integrated circuit
3 further comprises a counter that produces the digital value; wherein the counter is
4 configured to increase and decrease the digital value during an initialization period
5 depending on the relationship of the distributed reference voltage and the nominal
6 reference voltage, and the digital value remains constant during an operational
7 period following the initialization period.

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9 **24.** (original): An integrated circuit as recited in claim 17, further
10 comprising a capacitive charge pump that controls the gain of the reference
11 voltage driver.

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13 **25.** (Previously presented): An integrated circuit as recited in claim 17,
14 wherein the integrated circuit is a memory device that further comprises a plurality
15 of memory storage cells, each memory storage cell of the plurality of memory
16 storage cells coupled to at least one data receiver of the one or more data receivers
17 to store data received therefrom.

18
19 **26.** (Previously presented): An integrated circuit as recited in claim 17,
20 further comprising:

21 a charge pump that produces a control voltage to establish the variable gain
22 of the reference voltage driver;

23 wherein the charge pump is responsive to the feedback signal to increase
24 and decrease the variable gain.

1 **27.** (previously presented): An integrated circuit as recited in claim 17,
2 wherein the compensated reference voltage is distributed over impedance-matched
3 conductors to form the distributed reference voltage at the one or more data
4 receivers and at the feedback receiver.

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6 **28.** (previously presented): An integrated circuit as recited in claim 17,
7 wherein the feedback component incorporates a low-pass filter.

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9 **29.** (previously presented): An integrated circuit as recited in claim 17,
10 wherein the one or more data receivers comprise a plurality of the data receivers,
11 and wherein the distributed reference voltage is routed similarly to each of the data
12 receivers to result in similar degradation of the distributed reference voltage at
13 each of the data receivers.

14
15 **30.** (previously presented): An integrated circuit as recited in claim 17,
16 wherein the distributed reference voltage is routed similarly to the data and
17 feedback receivers to result in similar degradation of the distributed reference
18 voltage at the data and feedback receivers.

1 **31.** (Previously presented): An integrated circuit as recited in claim 17,
2 wherein the distributed reference voltage is routed similarly to the data and
3 feedback receivers to result in similar degradation of the distributed reference
4 voltage at the data and feedback receivers; and

5 wherein the feedback receiver incorporates a low-pass filter that does not
6 significantly affect the input characteristics of the feedback receiver.

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8 **32.** (original): An integrated circuit as recited in claim 17, wherein the
9 integrated circuit is a memory device that further comprises a plurality of memory
10 storage cells.
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1 33. (previously presented): An integrated circuit, comprising:
2 a plurality of data receivers that evaluate corresponding data signals relative
3 to a distributed reference voltage;
4 a feedback receiver that evaluates the distributed reference voltage relative
5 to a nominal reference voltage to produce a feedback signal;
6 a reference voltage driver that produces a compensated reference voltage;
7 wherein the compensated reference voltage is routed on the integrated
8 circuit to form the distributed reference voltage at the data and feedback receivers,
9 and the input characteristics of the data and feedback receivers cause a voltage
10 change in the distributed reference voltage at each receiver relative to the
11 compensated reference voltage;
12 wherein the data and feedback receivers have similar input characteristics
13 so that said relative voltage change in the distributed reference voltage is
14 approximately the same at each of the data and feedback receivers;
15 wherein the reference voltage driver includes an increment/decrement
16 component that produces a digital value in response to the feedback signal,
17 wherein the increment/decrement component is configured to increment and
18 decrement the digital value depending on the relationship of the distributed
19 reference voltage and the nominal reference voltage as indicated by the feedback
20 signal; and
21 wherein the reference voltage driver has a variable gain that is established
22 by the digital value.
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1 **34.** (original): An integrated circuit as recited in claim 33, wherein the
2 compensated reference voltage is distributed over impedance-matched conductors
3 to form the distributed reference voltage at the data and feedback receivers.
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5 **35.** (original): An integrated circuit as recited in claim 33, wherein the
6 increment/decrement component is enabled during an initialization period and the
7 digital value remains constant during a subsequent operational period.
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9 **36.** (original): An integrated circuit as recited in claim 33, further
10 comprising a register that is configurable to store the digital value and to provide
11 the digital value to the reference voltage driver.
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13 **37.** (previously presented): An integrated circuit as recited in claim 33,
14 further comprising a register that is configurable to store the digital value and to
15 provide the digital value to the reference voltage driver, wherein the register is
16 readable and writable.
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18 **38.** (original): An integrated circuit as recited in claim 33, further
19 comprising a digitally controllable variable resistor that controls the gain of the
20 reference voltage driver.
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22 **39.** (original): An integrated circuit as recited in claim 33, wherein the
23 feedback receiver comprises a low-pass filter that does not significantly affect the
24 input characteristics of the feedback receiver.
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1 **40.** (original): An integrated circuit as recited in claim 33, wherein the
2 distributed reference voltage is routed similarly to the data and feedback receivers
3 so that said relative voltage change in the distributed reference voltage is
4 approximately the same at each of the data and feedback receivers.

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6 **41.** (original): An integrated circuit as recited in claim 33, wherein:
7 the distributed reference voltage is routed similarly to the data and feedback
8 receivers so that said relative voltage change in the distributed reference voltage is
9 approximately the same at each of the data and feedback receivers; and
10 the feedback receiver comprises a low-pass filter that does not significantly
11 affect the input characteristics of the feedback receiver.

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13 **42.** (original): An integrated circuit as recited in claim 33, wherein the
14 integrated circuit is a memory device that further comprises a plurality of memory
15 storage cells.
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1 **43.** (Previously presented): An integrated circuit, comprising:
2 receiver means for evaluating a plurality of data signals relative to a
3 distributed reference voltage;
4 feedback means for evaluating the distributed reference voltage relative to a
5 nominal reference voltage to produce a feedback signal;
6 driver means having a variable gain for producing a compensated reference
7 voltage;
8 routing means for routing the compensated reference voltage on the
9 integrated circuit to form the distributed reference voltage at the receiver and
10 feedback means;
11 wherein the input characteristics of the receiver and feedback means cause
12 a voltage change in the distributed reference voltage at the receiver and feedback
13 means relative to the compensated reference voltage;
14 wherein the receiver and feedback means have similar input characteristics
15 so that said relative voltage change in the distributed reference voltage is
16 approximately the same at each of the receiver and feedback means; and
17 gain control means for controlling the gain of the driver means in response
18 to the feedback signal so that the distributed reference voltage is approximately
19 equal to the nominal reference voltage.

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21 **44.** (original): An integrated circuit as recited in claim 43, wherein the
22 gain control means comprises a counter that produces a digital value, wherein the
23 counter is responsive to the feedback to increment and decrement the digital value.
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1 **45.** (previously presented): An integrated circuit as recited in claim 43,
2 wherein the gain control means comprises a register that is configurable to store a
3 digital value, and wherein the variable gain of the driver means is responsive to
4 the digital value.

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6 **46.** (previously presented): An integrated circuit as recited in claim 43,
7 wherein the gain control means comprises a register that is configurable to store a
8 digital value, the variable gain of the driver means is responsive to the digital
9 value, and the register is readable and writable.

1 47. (previously presented): An integrated circuit, comprising:
2 receiver means for evaluating a plurality of data signals relative to a
3 distributed reference voltage;
4 feedback means for evaluating the distributed reference voltage relative to a
5 nominal reference voltage to produce a feedback signal;
6 driver means having a variable gain for producing a compensated reference
7 voltage;
8 routing means for routing the compensated reference voltage on the
9 integrated circuit to form the distributed reference voltage at the receiver and
10 feedback means;
11 wherein the input characteristics of the receiver and feedback means cause
12 a voltage change in the distributed reference voltage at the receiver and feedback
13 means relative to the compensated reference voltage;
14 wherein the receiver and feedback means have similar input characteristics
15 so that said relative voltage change in the distributed reference voltage is
16 approximately the same at each of the receiver and feedback means; and
17 gain control means for controlling the gain of the driver means in response
18 to the feedback signal so that the distributed reference voltage is approximately
19 equal to the nominal reference voltage;
20 wherein the compensated reference voltage is distributed over impedance-
21 matched conductors to form the distributed reference voltage at the receiver and
22 feedback means.

1 **48.** (original): An integrated circuit as recited in claim 43, wherein the
2 gain control means is enabled during an initialization period to adjust the gain of
3 the driver means, wherein the gain control means is configured to maintain the
4 gain of the driver means constant during a subsequent operational period.

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6 **49.** (original): An integrated circuit as recited in claim 43, wherein the
7 gain control means comprises a digitally controllable variable resistor.

8
9 **50.** (original): An integrated circuit as recited in claim 43, wherein the
10 distributed reference voltage is routed similarly to the receiver and feedback
11 means so that said relative voltage change in the distributed reference voltage is
12 approximately the same at each of the receiver and feedback means.

13
14 **51.** (previously presented): An integrated circuit as recited in claim 43,
15 wherein:

16 the distributed reference voltage is routed similarly to the receiver and
17 feedback means so that said relative voltage change in the distributed reference
18 voltage is approximately the same at each of the receiver and feedback means; and

19 the feedback means comprises a low-pass filter that does not significantly
20 affect the input characteristics of an op-amp thereof.

21
22 **52.** (original): An integrated circuit as recited in claim 43, wherein the
23 integrated circuit is a memory device that further comprises a plurality of memory
24 storage cells.

1 **53.** (previously presented): A memory device comprising:
2 a plurality of memory storage cells that are capable of storing data;
3 a plurality of data receivers that evaluate binary data signals with reference
4 to a distributed reference voltage and that are coupled to the plurality of memory
5 storage cells;
6 a feedback receiver that evaluates the distributed reference voltage relative
7 to a nominal reference voltage to produce a feedback signal;
8 a reference voltage driver that produces a compensated reference voltage;
9 wherein the compensated reference voltage is routed on the memory device
10 to form the distributed reference voltage at the data and feedback receivers, and
11 the input characteristics of the data and feedback receivers cause a voltage change
12 in the distributed reference voltage at each receiver relative to the compensated
13 reference voltage;
14 wherein the data and feedback receivers have substantially similar input
15 characteristics so that said relative voltage change in the distributed reference
16 voltage is approximately the same at each of the data and feedback receivers; and
17 wherein the reference voltage driver has a variable gain that is configurable
18 to increase in response to the feedback signal when the distributed reference
19 voltage is less than the nominal reference voltage and to decrease in response to
20 the feedback signal when the distributed reference voltage is greater than the
21 nominal reference voltage.

1 **54.** (Previously presented): A memory device comprising:
2 a plurality of memory storage cells that are capable of storing data;
3 a plurality of data receivers that evaluate binary data signals with reference
4 to a distributed reference voltage and that are coupled to the plurality of memory
5 storage cells;
6 a feedback receiver that evaluates the distributed reference voltage relative
7 to a nominal reference voltage to produce a feedback signal;
8 a reference voltage driver that produces a compensated reference voltage;
9 wherein the compensated reference voltage is routed on the memory device
10 to form the distributed reference voltage at the data and feedback receivers, and
11 the input characteristics of the data and feedback receivers cause a voltage change
12 in the distributed reference voltage at each receiver relative to the compensated
13 reference voltage;
14 wherein the data and feedback receivers have similar input characteristics
15 so that said relative voltage change in the distributed reference voltage is
16 approximately the same at each of the data and feedback receivers; and
17 wherein the reference voltage driver has a variable gain that is configurable
18 to increase in response to the feedback signal when the distributed reference
19 voltage is less than the nominal reference voltage and to decrease in response to
20 the feedback signal when the distributed reference voltage is greater than the
21 nominal reference voltage;
22 wherein the compensated reference voltage is distributed over impedance-
23 matched conductors to form the distributed reference voltage at the data and
24 feedback receivers.
25

1 **55.** (original): A memory device as recited in claim 53, wherein the
2 variable gain of the reference voltage driver is controlled by a digital value, the
3 integrated circuit further comprising a register that is configurable to store the
4 digital value and to provide the digital value to the reference voltage driver.

5
6 **56.** (previously presented): A memory device as recited in claim 53,
7 wherein the variable gain of the reference voltage driver is controlled by a digital
8 value, and the integrated circuit further comprises a register that is configurable to
9 store the digital value and to provide the digital value to the reference voltage
10 driver; and wherein the register is readable and writable.

11
12 **57.** (original): A memory device as recited in claim 53, wherein the gain
13 of the reference voltage driver remains constant during an operational period that
14 follows an initialization period.

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16 **58.** (original): A memory device as recited in claim 53, wherein the
17 feedback receiver comprises a low-pass filter that does not significantly affect the
18 input characteristics of the feedback receiver.
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1 **59.** (original): A memory device as recited in claim 53, wherein:

2 the distributed reference voltage is routed similarly to the data and feedback
3 receivers so that said relative voltage change in the distributed reference voltage is
4 approximately the same at each of the data and feedback receivers; and

5 the feedback receiver comprises a low-pass filter that does not significantly
6 affect the input characteristics of the feedback receiver.

7
8 **60.** (previously presented): A method comprising:

9 amplifying a nominal voltage by a variable gain to produce a compensated
10 reference voltage;

11 routing the compensated reference voltage over approximately impedance-
12 matched resistive conductors to form a distributed voltage;

13 evaluating a plurality of signals relative to the distributed voltage;

14 evaluating the nominal voltage relative to the distributed voltage;

15 increasing the variable gain when the distributed voltage is less than the
16 nominal voltage; and

17 decreasing the variable gain when the distributed voltage is greater than the
18 nominal voltage.

19
20 **61.** (previously presented): A method as recited in claim 60, wherein

21 the amplifying comprises amplifying the nominal voltage by a variable gain that
22 is established by a digital value.

1 **62.** (original): A method as recited in claim 60, further comprising:
2 maintaining the variable gain at a constant value during an operational
3 period following an initialization period.

4
5 **63.** (previously presented): An integrated circuit, comprising:
6 a reference voltage driver that has a variable gain and produces a
7 compensated reference voltage; and

8 a plurality of receivers having substantially similar input characteristics that
9 evaluate signals relative to a distributed reference voltage, a particular receiver of
10 the plurality of receivers capable of evaluating a nominal reference voltage signal
11 relative to the distributed reference voltage to produce a feedback signal;

12 wherein the compensated reference voltage is distributed to form the
13 distributed reference voltage, and the distributed reference voltage is degraded
14 relative to the compensated reference voltage; and

15 wherein the reference voltage driver is responsive to the feedback signal
16 such that the variable gain increases when the distributed reference voltage is less
17 than the nominal reference voltage signal and decreases when the distributed
18 reference voltage is greater than the nominal reference voltage signal.

19
20 **64.** (previously presented): An integrated circuit as recited in claim 63,
21 wherein the particular receiver is useable during an initialization period to evaluate
22 the nominal reference voltage signal relative to the distributed reference voltage to
23 produce the feedback signal and is unused during an operational period.

1 **65.** (previously presented): An integrated circuit as recited in claim 63,
2 wherein the particular receiver is useable during an initialization period to evaluate
3 the nominal reference voltage signal relative to the distributed reference voltage to
4 produce the feedback signal and is useable during an operational period to
5 evaluate a data signal relative to the distributed reference voltage.

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7 **66.** (previously presented): An integrated circuit as recited in claim 63,
8 wherein the compensated reference voltage is distributed over impedance-matched
9 conductors to form the distributed reference voltage at the plurality of receivers.

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11 **67.** (previously presented): An integrated circuit as recited in claim 63,
12 wherein the substantially similar input characteristics cause a voltage change in
13 the distributed reference voltage at each receiver relative to the compensated
14 reference voltage that is approximately the same at each receiver of the plurality of
15 receivers.

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17 **68.** (previously presented): An integrated circuit as recited in claim 63,
18 wherein the particular receiver includes a low-pass filter that does not significantly
19 affect input characteristics of the particular receiver.

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21 **69.** (previously presented): An integrated circuit as recited in claim 63,
22 further comprising memory storage cells.
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1 70. (previously presented): An integrated circuit as recited in claim 63,
2 wherein the variable gain of the reference voltage driver is controlled by a digital
3 value.

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5 71. (previously presented): An integrated circuit as recited in claim 63,
6 further comprising a register that is configurable to store a digital value; wherein
7 the variable gain of the reference voltage driver is controllable by the digital value
8 of the register.

9
10 72. (previously presented): An integrated circuit as recited in claim 63,
11 wherein the reference voltage driver includes a counter that can change the
12 variable gain of the reference voltage driver responsive to the feedback signal.

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14 73. (previously presented): An integrated circuit as recited in claim 63,
15 further comprising a charge pump that produces a control voltage to establish the
16 variable gain of the reference voltage driver; wherein the charge pump is
17 responsive to the feedback signal to cause the variable gain to increase or
18 decrease.